REMARKS

Status of the Claims

Claims 1, 2 and 4-52 were pending.

Claims 1, 2, 4-8, 15 and 18-52 were rejected.

Please **amend** claims 6, 7, 38 and 39 **add** 53, 54, 55, and **cancel** claims 50, 51, 52.

It is believed that the remarks laid out herein below attend to all rejections and further issues raised in the pending office action dated 8 March 2007.

Claim Rejections

Claim Rejections Under 35USC112

Claims 6, 7, 38 and 39 are rejected under 35USC112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Amends have been made to claims 6, 7, 38 and 39 and the claims are no longer indefinite.

Claim Rejections – 35 U.S.C. § 103(a)

Claims 1, 2, 4, 5, 8, 15, 18-23, 32-37, 40, 41 and 49-52 were rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over U.S. Patent No. 7,092,352 (Shattil).

For the purpose of the following discussion, the Examiner is respectfully reminded of the basic considerations which apply to obviousness rejections.

When applying 35 U.S.C. §103, the following tenets of patent law must be adhered to:

(A) The claimed invention must be considered as a whole;

(B) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination;

(C) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and

(D) Reasonable expectation of success is the standard with which obviousness is determined. MPEP §2141.01, *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1134 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986).

Claim 1, includes the following features:

> a receiver receiving a plurality of digital signal streams, at least one of the plurality of digital signal streams being coupled to another of the plurality of digital signal streams;
>
> a domain transformer for transforming sub-blocks of at least one of the plurality of the digital signal streams from an original domain into a lower complexity domain, wherein *each sub-block includes less digital signal stream samples than a block, wherein a block includes enough samples to exceed joint filter time sample spans of the plurality of digital signal streams*;
>
> a processor for joint processing of the transformed sub-blocks of the plurality of digital signal streams, each of the joint processed digital signal stream sub-blocks being influenced by other digital signal streams sub-blocks; and
>
> *an inverse transformer for inverse transforming the joint processed signal streams sub-blocks back to the original domain.*

The Examiner stated that Shattil includes "an inverse transformer for inverse transforming the joint processed signal streams sub-blocks back to the original domain (505 in Fig. 5B, wherein output of the element is back to the time domain)."

Applicants respectfully disagree. The Examiner appears to have been misled by sloppy notation of the Shattil patent. The block 505 of Shattil is a decoder, and does not provide a frequency to time transformation. Rather, the decoder merely decodes frequency components. Therefore, Shattil does not teach or suggest an inverse

transformer for inverse transforming the joint processed signal streams sub-blocks back to the original domain. It is not an obvious extension to add an inverse transformation to the teachings of Shattil.

Shattil provides a communication system that is adapted to transmit a plurality of data symbols $s_{1n}(t)$ to $s_{Mn}(t)$ between a transmitter array and a receiver array (column 6, line 65 to column 7, line1.). For the notation of Shattil, *m* (m=1, ..., M) represents a chain or transmit antenna, *n* (n=1, ... N) represents a frequency index and t represents time.

For a better understanding of the notation of Shattil, please refer to Figures 3A, 3B, 4A and 4B of Shattil. Figure 3A shows a frequency-to-time converter 310 that has N frequency domain inputs $\{s_{m1}(t), s_{m2}(t), \ldots s_{mN}(t)\}$ and an a time domain output $s_m(t)$. Figure 4A shows a time-to-frequency converter 410 that has a time domain input $r_m(t)$ and N frequency domain outputs $\{r_{m1}(t), r_{m2}(t), \ldots r_{mN}(t)\}$. According to the notation of Shattil, f_n (n=1, ... N) (see col. 7, lines 5,6 of Shattil) indicates the frequency index or carrier frequency, and t indicates time for both the frequency and the time domain representations.

Figure 4B shows a time-to-frequency transformation and a decoder – analogous to the configuration of Figure 5B. Here, Shattil depicts the input as $r_m(t)$, and the transformed and decoded outputs as $\{r_{m1}(t), r_{m2}(t), \ldots r_{mN}(t)\}$. The frequency transformation is indicated as described above, by including the index number (n=1, ... N).

The Examiner has been reasonably confused by Figure 5B because Shattil is not consistent in the use of notation. Figures 5A and 5B show a weight-and-sum circuit that can be used to cancel and/or separate interfering data symbols. In these figures, Shattil changes the notation of the outputs of the time-to-frequency transformation (inputs to the weight and sum circuits) to be $r_{Mn}(f_n)$. Even worse, Figure 5B uses both types of notation (*n* and f_n) to indicate frequency. More specifically, Shattil shows the output of the combiner 503 as $s'_{m'}(f_n)$ – dropping the frequency index (*n*). The output

of the decoder 505 switches back to the notation of Figures 3A, 3B, 4A, 4B again including the time component. The output of the decoder 505 $s'_{m'n}(t)$ includes the chain number m', the frequency index n, and the time component t. Clearly, the output of the decoder includes the frequency index (n) – indicating the signals are still in the frequency domain, and no transformation has taken place. Shattil describes the component 505 as an optional decoder that may perform decoding as necessary, and that the decoding may include channel estimation (column 9, lines 53-54). There is absolutely no discussion suggesting that the decoder 505 provides a domain transformation.

Additionally, Shattil does not teach of suggest restricting the size of the sub-blocks. The Examiner stated "One skilled in the art would further recognize that reducing the number of samples reduces the computation load by a processor. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to recognize that the system of Shattil produces subsamples from a sample or block that includes enough samples to exceed joint filtering time sample spans of the plurality of digital signal streams, for the purpose of reducing computation load by reducing the number of samples for further processing". Applicants respectfully disagree. Actually, the computation is more complex – that is, computations are more efficient in the transform domain with larger block sizes. The Examiner is directed to the equations of pages 24-27 of applicant's specification. The computation of these equations is greater for smaller block sizes. That is, as N increases, the efficiency of calculation improves. The computations are increased to obtain a decrease in latency.

Claim 1 is patentable over the cited prior art.

Claims 2, 4-25, 27-31 are directly or indirectly dependent on claim 1. Therefore, claims 2, 4-25, 27-31 are patentable over the cited prior art. Additionally, these claims rely on sub-blocking which is not taught by the cited references.

Claim 2 includes limiting a block including enough digital signal stream samples that transforming and processing blocks of the plurality of digital signal

streams does not introduce distortion. The Examiner stated that Shattil teaches a cancellation circuit and hence one skilled in the art would recognize that the circuit cancels distortion or noise. However, claim 2 is directed to a block size which is not taught or suggested by Shattil. Noise cancellation can be achieved through many different means – not necessarily through limiting distortion by block size selection.

Claim 7 was only addressed in the 35USC112, second paragraph rejection. Therefore, claim 7 is patentable over the cited references.

The Examiner has indicated that claims 9-14, 16 and 17 are allowable – the base claims are allowable as well.

Independent claims 32, 33, 34, 35, 49 all include a limitation on the size of blocks, and then further specifies that processing is on sub-blocks that include less samples than the blocks. These independent claims also include both the domain transformation and the inverse domain transformation. None of the cited references individually or in combination teach or suggest these features. Therefore, claims 32, 33, 34, 35, 49 are patentable.

Claims 36-49 are directly or indirectly dependent on claim 35. Therefore claims 36-49 are patentable.

Claim 10, includes the feature that the diagonal elements of the sub-block processing matrices are adaptively selected. This feature is not taught by the cited prior art. Therefore, claim 10 is additionally patentable over the cited references.

Amended claim 35, and new claims 53, 54, 55 include features similar to the claim combination of old claims 1, 8 and 12 which the Examiner has indicated are allowable.

CONCLUSION

For the reasons given above, and after careful review of the cited reference, applicant respectfully submits that Shattil does not result in, teach or suggest applicant's claimed invention.

In view of the above Remarks, applicant has addressed all issues raised in the Office Action dated 08 March 2007, and respectfully solicits a Notice of Allowance for claims 1, 2, 4-25, 27-49, 53-55. Should any issues remain, the Examiner is encouraged to telephone the undersigned attorney.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Respectfully submitted,

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